Rump Session: Advanced Silicon Technology Foundry Access Options for DoD Research

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Daunting challenge of fab access for U. S. universities

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IN THE CITY OF NEW YORK

Requirements

- U. S. universities must have access to semiconductor processing technologies to validate designs and innovate
- General needs require access to:
  - General CMOS technology nodes
    - Bleeding edge technology to explore latest issues: variability, highest frequency performance
    - More general CMOS node to explore mixed technologies and alternate applications
  - Specialized needs to SiGe, MEMS
- In some cases, in which large systems are explored, large silicon areas are required

Fabrication alternatives for U. S. universities

5 mm x 5 mm 0.13μm CMOS

- MOSIS
  - $72,500 for university pricing (TSMC)
- Europractice
  - 27,400 Euros ($34,689) (UMC)
- TAPO with 1/3 pricing (on DoD funded programs only)
  - $43,000 (IBM)
- CMP
  - 33,250 Euros ($42,106) (STM)

MOSIS has a 5 mm x 5 mm minimum. Both CMP and Europractice allow smaller dice to be fabricated with almost linear cost scaling.

Fabrication alternatives for U. S. universities

12 mm^2 65-nm CMOS

- MOSIS
  - $99,000 (IBM)
- Europractice
  - Not available.
- TAPO with 1/3 pricing (on DoD funded programs only)
  - ~ $60,000 (IBM)
- CMP
  - 93,000 Euros ($117,900) (STM)

MOSIS has a 12 mm^2 minimum. CMP allows smaller dice to be fabricated with almost linear cost scaling.

Other programs

- SRC offers a match for MOSIS fabricated runs but this is capped at $24K. Must be an SRC GRC-funded project. Very limited funds. Also, revised minimums and pricing (for SRC projects only)
  - IBM 130nm (8RF-DM) (min) 4 sq mm $10K
    - Europractice: $3790 (but only a 2.3 mm^2 block); CMP: $11,557
  - IBM 90nm (9SF, 9RF/LP) (min) 4 sq mm $25K
    - Europractice: $9160 (but only a 3.5 mm^2 block); CMP: $25,327
  - IBM 65nm (10SF, 10LP) (min) 4 sq mm $48K
    - Europractice: Not available; CMP: $48,127
- Both UMC and TSMC offer free shuttle runs to U. S. universities on a limited basis.
  - Complex relationship with the foundries with sticky IP arrangements and lots of trips to Taiwan.
- Some U. S. faculty with ties to China are getting free fab through SMIC (Shanghai), which offers technologies down to 65-nm CMOS

International competitive landscape

- Taiwanese universities have almost “all you can eat” access to TSMC and UMC foundry.
- Chinese universities have a similar relationship with SMIC, many involved with large government “competitiveness” projects – “replacement” for Intel microprocessor
- European Union subsidizes Europractice, but until recently, U. S. has had almost the same access as Europeans (this may change).

Opportunities…

- TAPO program is fully funded for U. S. universities participating in DoD-funded (or DARPA-funded) research on a vetted basis.
- Are there opportunities to leverage the Albany Nanotech facility? NYS has already invested billions in this enterprise.
- Bottom line: There needs to be a solution here that is on a par with our Asian competitors.